OPAx277 High Precision Operational Amplifiers

1 Features

- Ultralow Offset Voltage: 10 μV
- Ultralow Drift: ±0.1 μV/°C
- High Open-Loop Gain: 134 dB
- High Common-Mode Rejection: 140 dB
- High Power Supply Rejection: 130 dB
- Low Bias Current: 1-nA maximum
- Wide Supply Range: ±2 V to ±18 V
- Low Quiescent Current: 800 μA/amplifier
- Single, Dual, and Quad Versions
- Replaces OP-07, OP-77, and OP-177

2 Applications

- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gage Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

3 Description

The OPAx277 series precision operational amplifiers replace the industry standard OP-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultralow offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications, for maximum design flexibility.

OPAx277 series operational amplifiers operate from ±2-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPAx277 series is specified for real-world applications; a single limit applies over the ±5-V to ±15-V supply range. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±20 μV maximum) is so low, user adjustment is usually not required. However, the single version (OPA277) provides external trim pins for special applications.

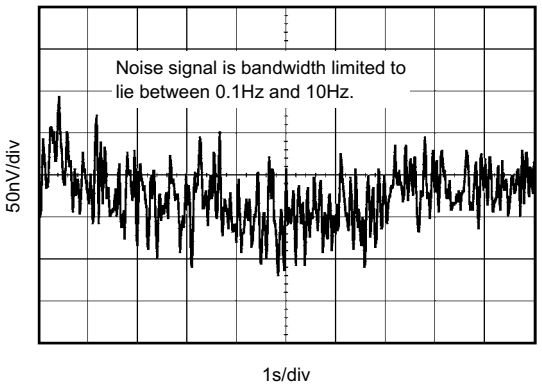
OPA277 operational amplifiers are easy to use and free from phase inversion and the overload problems found in some other operational amplifiers. They are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA277 OPA2277	VSON (8)	4.00 mm × 4.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
OPA4277	SOIC (14)	3.91 mm × 8.65 mm
	PDIP (14)	6.35 mm × 19.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

0.1 Hz to 10 Hz Noise



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

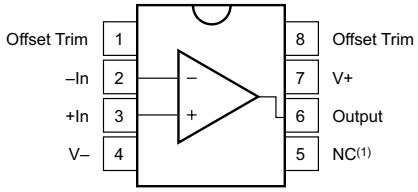
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2005) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

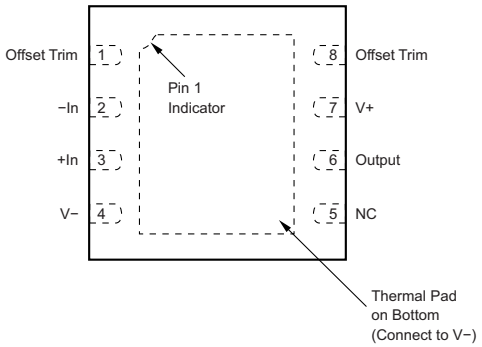
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5 Pin Configuration and Functions

OPA277 P and D Packages
8-Pin PDIP and SOIC
Top View



OPA277 DRM Package
8-Pin VSON
Top View

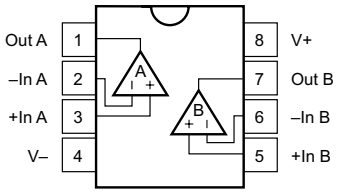


Pin Functions: OPA277

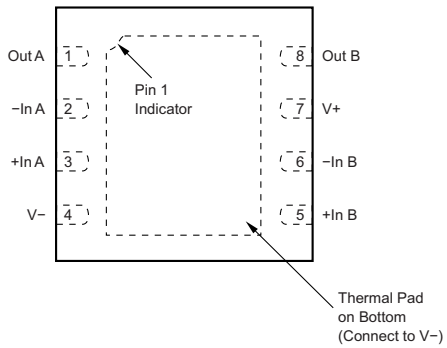
PIN		I/O	DESCRIPTION
NO.	NAME		
1	Offset Trim	I	Input offset voltage trim (leave floating if not used)
2	–In	I	Inverting input
3	+In	I	Noninverting input
4	V–	—	Negative (lowest) power supply
5	NC	—	No internal connection (can be left floating)
6	Output	O	Output
7	V+	—	Positive (highest) power supply
8	Offset Trim	—	Input offset voltage trim (leave floating if not used)

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OPA2277 P and D Packages
8-Pin PDIP and SOIC
Top View



OPA2277 DRM Package
8-Pin VSON
Top View

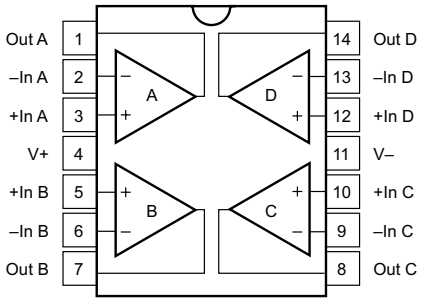


Pin Functions: OPA2277

PIN			I/O	DESCRIPTION
NAME	PDIP, SOIC NO.	DFN NO.		
Out A	1	1	O	Output channel A
–In A	2	2	I	Inverting input channel A
+In A	3	3	I	Noninverting input channel A
V–	4	4	—	Negative (lowest) power supply
+In B	5	5	I	Noninverting input channel B
–In B	6	6	I	Inverting input channel B
Out B	7	8	O	Output channel B
V+	8	7	—	Positive (highest) power supply

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OPA4277 P and D Packages
14 Pins PDIP and SOIC
Top View



Pin Functions: OPA4277

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Out A	O	Output channel A
2	–In A	I	Inverting input channel A
3	+In A	I	Noninverting input channel A
4	V+	—	Positive (highest) power supply
5	+In B	I	Noninverting input channel B
6	–In B	I	Inverting input channel B
7	Out B	O	Output channel B
8	Out C	O	Output channel C
9	–In C	I	Inverting input channel C
10	+In C	I	Noninverting input channel C
11	V–	—	Negative (lowest) power supply
12	+In D	I	Noninverting input channel D
13	–In D	I	Inverting input channel D
14	Out D	O	Output channel D

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)		36	V
Input voltage	(V–) –0.7	(V+) +0.7	V
Output short-circuit (2)	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature		300	°C
Storage temperature, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)	4 (±2)	30 (±15)	36 (±18)	V
Specified temperature	–40		+85	°C

6.4 Thermal Information for OPA277

THERMAL METRIC (1)		OPA277			UNIT
		P (PDIP)	D (SOIC)	DRM (VSON)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.2	110.1	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.4	52.2	41.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.4	52.3	16.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.4	10.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.3	51.5	16.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information for OPA2277

THERMAL METRIC (1)		OPA2277			UNIT
		P (PDIP)	D (SOIC)	DRM (VSON)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	107.4	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.0	45.8	36.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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Thermal Information for OPA2277 (continued)

THERMAL METRIC[1]		OPA2277			UNIT
		P (PDIP)	D (SOIC)	DRM (VSON)	
		8 PINS			
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	47.9	15.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.4	5.7	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.3	47.3	15.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	2.2	°C/W

6.6 Thermal Information for OPA4277

THERMAL METRIC[1]		OPA4277		UNIT
		D (SOIC)	P (PDIP)	
		14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.0	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	20.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.1	26.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics for OPAx277P, OPAx277U, and OPAx277xA

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
OFFSET VOLTAGE										
V_{OS}	Input Offset Voltage				±10	±20		±20	±50	µV
	Input Offset Voltage Over Temperature	OPA277P, U (high-grade, single)	T_A = –40°C to 85°C			±30				µV
		OPA2277P, U (high-grade, dual)				±50				
		All PA, UA, Versions							±100	
		AIDRM Versions								
dV_{OS}/dT	Input Offset Voltage Drift	OPA277P, U (high-grade, single)	T_A = –40°C to 85°C		±0.1	±0.15				µV/°C
		OPA2277P, U (high-grade, dual)			±0.1	±0.25				
		All PA, UA, AIDRM Versions						±0.15	±1	
	Input Offset Voltage: (all models)	vs Time			0.2			See [2]		µV/mo
		vs Power Supply (PSRR)	V_S = ±2 V to ±18 V		±0.3	±0.5		See [2]	±1	µV/V
			T_A = –40°C to 85°C			±0.5			±1	
	Channel Separation (dual, quad)		DC		0.1			See [2]		µV/V

(1) V_S = ±15 V
(2) Specifications are the same as OPA277P, U.

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Electrical Characteristics for OPAx277P, OPAx277U, and OPAx277xA (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			UNIT
				MIN	TYP(1)	MAX	MIN	TYP (1)	MAX	
INPUT BIAS CURRENT										
I_B	Input Bias Current		T_A = –40°C to 85°C		±0.5	±1		See (2)	±2.8	nA
						±2			±4	
I_{OS}	Input Offset Current		T_A = –40°C to 85°C		±0.5	±1		See (2)	±2.8	nA
						±2			±4	
NOISE										
	Input Voltage Noise, f = 0.1 to 10 Hz				0.22			See (2)		μV_{PP}
e_n	Input Voltage Noise Density	f = 10 Hz			12			See (2)		nV/√Hz
		f = 100 Hz			8			See (2)		
		f = 1 kHz			8			See (2)		
		f = 10 kHz			8			See (2)		
i_n	Current Noise Density, f = 1 kHz				0.2			See (2)		pA/√Hz
INPUT VOLTAGE RANGE										
V_{CM}	Common-Mode Voltage Range			(V–)+2		(V+)–2	See (2)		See (2)	V
CMRR	Common-Mode Rejection		V_{CM} = (V–) +2 V to (V+) –2 V	130	140		115	See (2)		dB
			T_A = –40°C to 85°C	128			115			
INPUT IMPEDANCE										
	Differential				100 || 3			See (2)		MΩ || pF
	Common-Mode		V_{CM} = (V–) +2 V to (V+) –2 V		250 || 3			See (2)		GΩ || pF
OPEN-LOOP GAIN										
A_{OL}	Open-Loop Voltage Gain		V_O = (V–)+0.5 V to (V+)–1.2 V, R_L = 10 kΩ		140			See (2)		dB
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	126	134		See (2)	See (2)		
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	126			See (2)			dB
			T_A = –40°C to 85°C							
FREQUENCY RESPONSE										
GBW	Gain-Bandwidth Product				1			See (2)		MHz
SR	Slew Rate				0.8			See (2)		V/µs
	Settling Time	0.1%	V_S = ±15 V, G = 1, 10-V Step		14			See (2)		µs
		0.01%			16			See (2)		
	Overload Recovery Time		V_{IN} × G = V_S		3			See (2)		µs
THD+N	Total Harmonic Distortion + Noise		1 kHz, G = 1, V_O = 3.5 Vrms		0.002%			See (2)		

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Electrical Characteristics for OPAx277P, OPAx277U, and OPAx277xA (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			UNIT
			MIN	TYP(1)	MAX	MIN	TYP (1)	MAX	
OUTPUT									
V_O	Voltage Output	R_L = 10 kΩ	(V–)+0.5		(V+)–1.2	See (2)		See (2)	V
		T_A = –40°C to +85°C	(V–)+0.5		(V+)–1.2	See (2)		See (2)	
		R_L = 2 kΩ	(V–)+1.5		(V+)–1.5	See (2)		See (2)	
		T_A = –40°C to +85°C	(V–)+1.5		(V+)–1.5	See (2)		See (2)	
I_{SC}	Short-Circuit Current			±35			See (2)		mA
C_{LOAD}	Capacitive Load Drive			See (3)					
Z_O	Open-loop output impedance	f = 1 MHz		40			See (2)		Ω
POWER SUPPLY									
V_S	Specified Voltage Range		±5		±15	See (2)		See (2)	V
	Operating Voltage Range		±2		±18	See (2)		See (2)	V
I_Q	Quiescent Current (per amplifier)	I_O = 0		±790	±825		See (2)	See (2)	µA
		T_A = –40°C to 85°C			±900			See (2)	
TEMPERATURE RANGE									
	Specified Range		–40		85	See (2)		See (2)	°C
	Operating Range		–55		125	See (2)		See (2)	°C

(3) See *Typical Characteristics*

6.8 Electrical Characteristics for OPAx277AIDRM

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	OPA277AIDRM OPA2277AIDRM			UNIT
				MIN	TYP(1)	MAX	
OFFSET VOLTAGE							
V_{0S}	Input Offset Voltage				±35	±100	µV
	Input Offset Voltage Over Temperature	OPA277P, U (high-grade, single)	T_A = –40°C to 85°C				µV
		OPA2277P, U (high-grade, dual)					
		All PA, UA, Versions					
		AIDRM Versions				±165	
dV_{0S}/dT	Input Offset Voltage Drift	OPA277P, U (high-grade, single)	T_A = –40°C to 85°C				µV/°C
		OPA2277P, U (high-grade, dual)					
		All PA, UA, AIDRM Versions			±0.15	±1	
	Input Offset Voltage: (all models)	vs Time			See (2)		µV/mo
		vs Power Supply (PSRR)	V_S = ±2 V to ±18 V		See (2)	±1	µV/V
			T_A = –40°C to 85°C			±1	
	Channel Separation (dual, quad)		DC		See (2)		µV/V

(1) V_S = ±15 V
(2) Specifications are the same as OPA277P, U.

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Electrical Characteristics for OPAx277AIDRM (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	OPA277AIDRM OPA2277AIDRM			UNIT
				MIN	TYP(1)	MAX	
INPUT BIAS CURRENT							
I_B	Input Bias Current		T_A = –40°C to 85°C			±2.8	nA
						±4	
I_{OS}	Input Offset Current		T_A = –40°C to 85°C			±2.8	nA
						±4	
NOISE							
	Input Voltage Noise, f = 0.1 to 10 Hz				See (2)		μV_{PP}
e_n	Input Voltage Noise Density	f = 10 Hz			See (2)		nV/√Hz
		f = 100 Hz			See (2)		
		f = 1 kHz			See (2)		
		f = 10 kHz			See (2)		
i_n	Current Noise Density, f = 1 kHz				See (2)		pA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-Mode Voltage Range			See (2)		See (2)	V
CMRR	Common-Mode Rejection		V_{CM} = (V–) +2 V to (V+) –2 V	115	See (2)		dB
			T_A = –40°C to 85°C	115			
INPUT IMPEDANCE							
	Differential				See (2)		MΩ || pF
	Common-Mode		V_{CM} = (V–) +2 V to (V+) –2 V		See (2)		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-Loop Voltage Gain		V_O = (V–)+0.5 V to (V+)–1.2 V, R_L = 10 kΩ		See (2)		dB
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	See (2)	See (2)		
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	See (2)			dB
			T_A = –40°C to 85°C				
FREQUENCY RESPONSE							
GBW	Gain-Bandwidth Product				See (2)		MHz
SR	Slew Rate				See (2)		V/µs
	Settling Time	0.1%	V_S = ±15 V, G = 1, 10-V Step		See (2)		µs
		0.01%			See (2)		
	Overload Recovery Time		V_{IN} × G = V_S		See (2)		µs
THD+N	Total Harmonic Distortion + Noise		1 kHz, G = 1, V_O = 3.5 Vrms		See (2)		
OUTPUT							
V_O	Voltage Output		R_L = 10 kΩ	See (2)		See (2)	V
			T_A = –40°C to +85°C	See (2)		See (2)	
			R_L = 2 kΩ	See (2)		See (2)	
			T_A = –40°C to +85°C	See (2)		See (2)	
I_{SC}	Short-Circuit Current				See (2)		mA
C_{LOAD}	Capacitive Load Drive						
Z_O	Open-loop output impedance		f = 1 MHz		See (2)		Ω

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Electrical Characteristics for OPAx277AIDRM (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	OPA277AIDRM OPA2277AIDRM			UNIT
			MIN	TYP(1)	MAX	
POWER SUPPLY						
V_S	Specified Voltage Range		See (2)		See (2)	V
	Operating Voltage Range		See (2)		See (2)	V
I_Q	Quiescent Current (per amplifier)	I_O = 0		See (2)	See (2)	μA
		T_A = –40°C to 85°C			See (2)	
TEMPERATURE RANGE						
	Specified Range		See (2)		See (2)	°C
	Operating Range		See (2)		See (2)	°C

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6.9 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

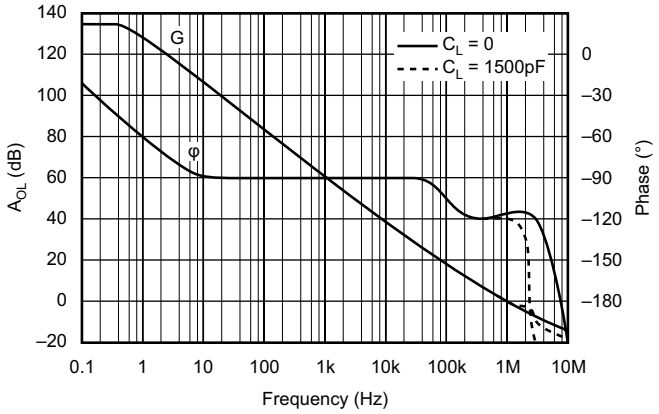


Figure 1. Open-Loop Gain and Phase vs Frequency

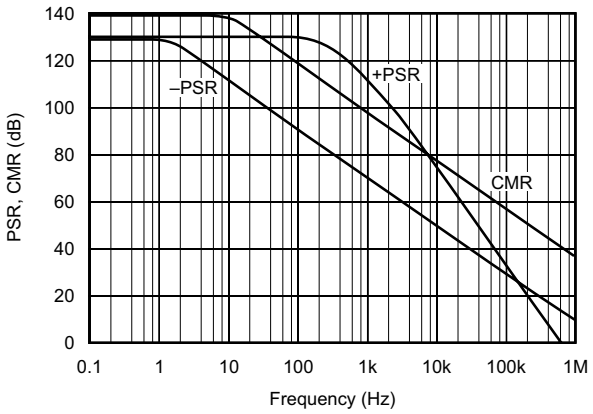


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

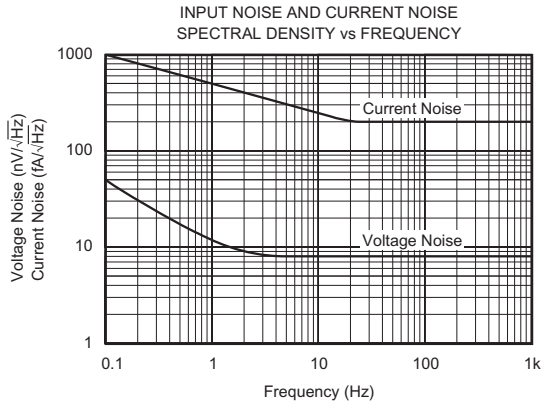


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency

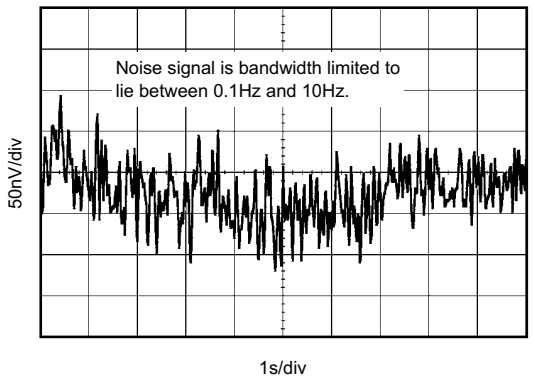


Figure 4. Input Noise Voltage vs Time

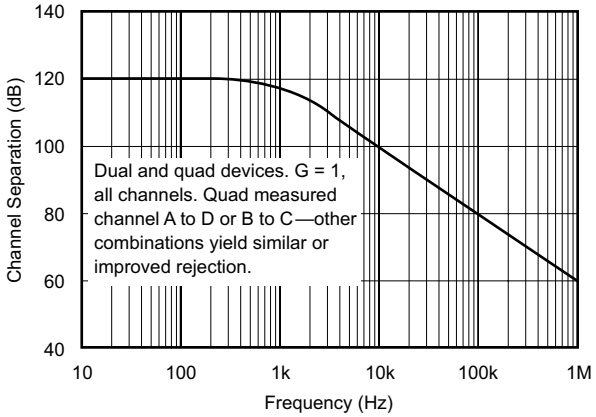


Figure 5. Channel Separation vs Frequency

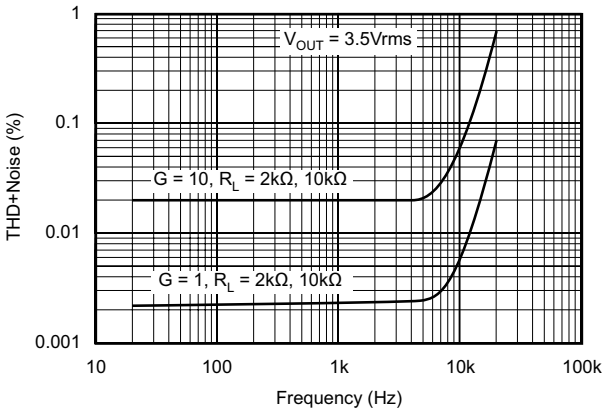


Figure 6. Total Harmonic Distortion + Noise vs Frequency

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

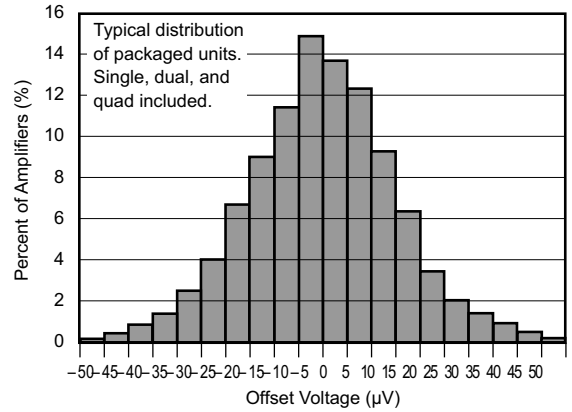


Figure 7. Offset Voltage Production Distribution

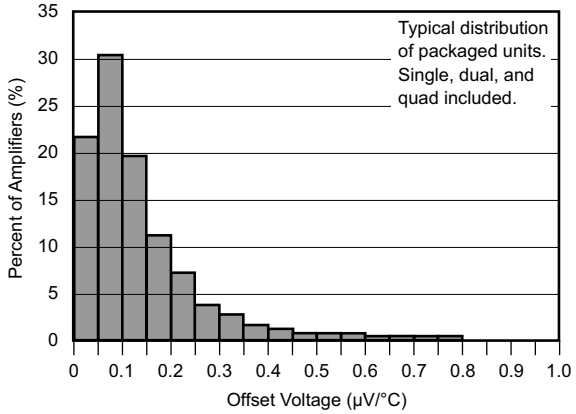


Figure 8. Offset Voltage Drift Production Distribution

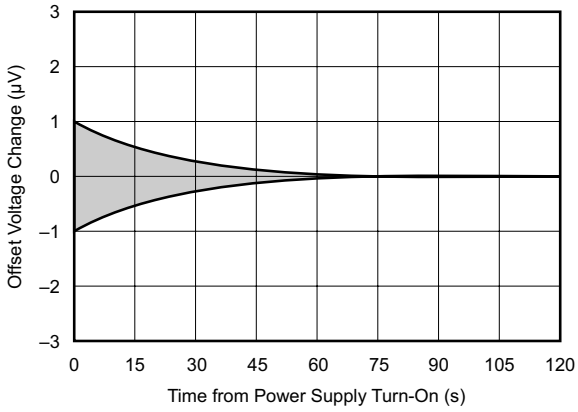


Figure 9. Warm-Up Offset Voltage Drift

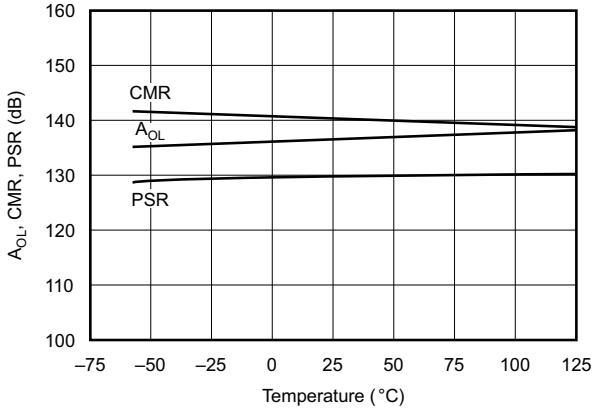


Figure 10. A_{OL}, CMR, PSR vs Temperature

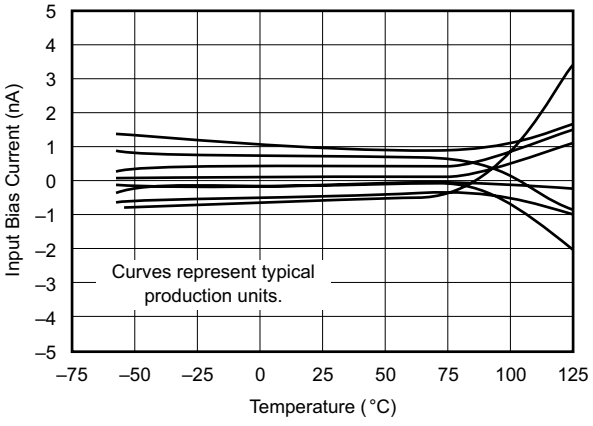


Figure 11. Input Bias Current vs Temperature

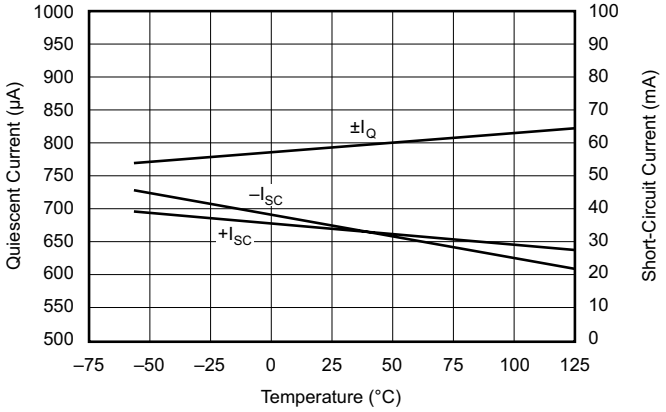


Figure 12. Quiescent Current and Short-Circuit Current vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

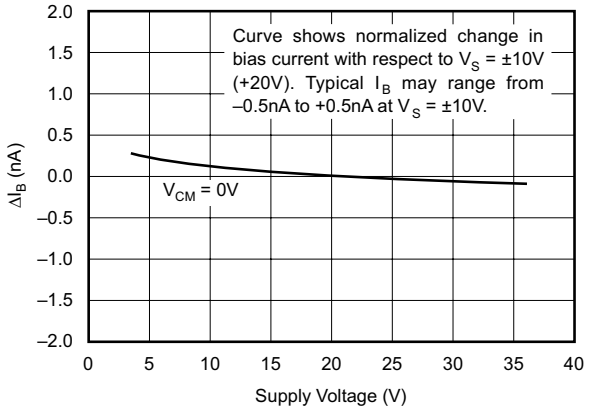


Figure 13. Change in Input Bias Current vs Power Supply Voltage

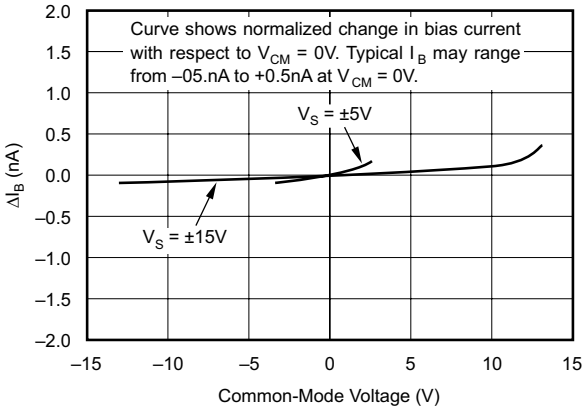


Figure 14. Change in Input Bias Current vs Common-Mode Voltage

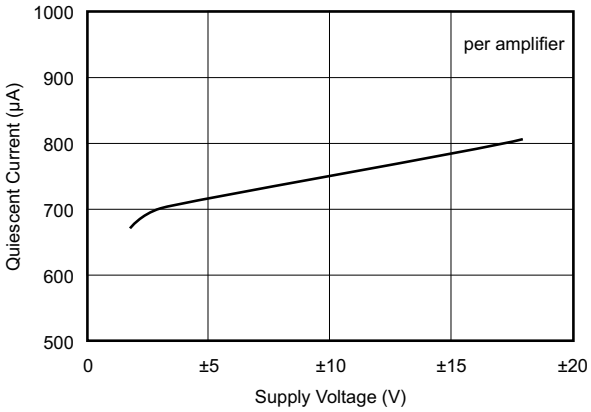


Figure 15. Quiescent Current vs Supply Voltage

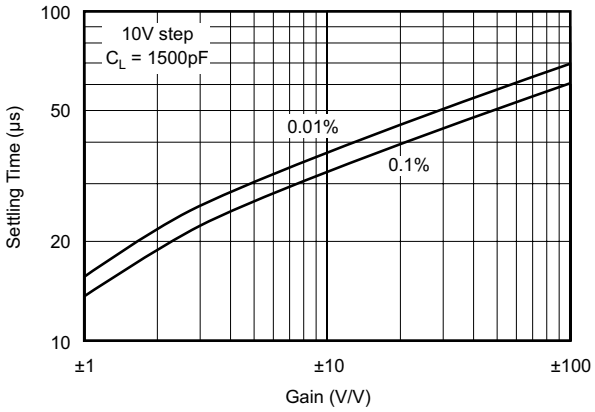


Figure 16. Settling Time vs Closed-Loop Gain

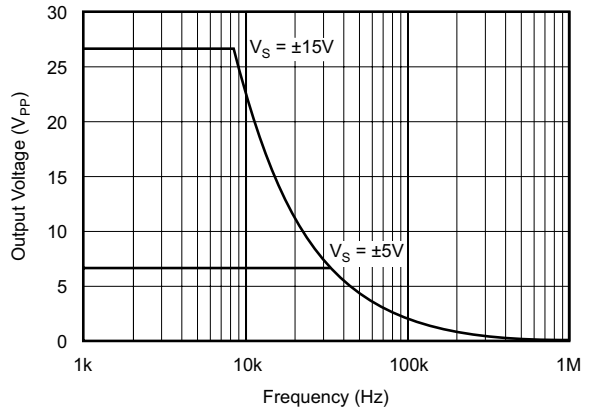


Figure 17. Maximum Output Voltage vs Frequency

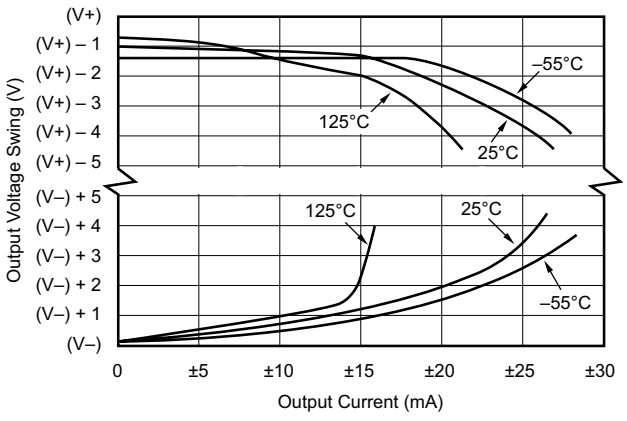


Figure 18. Output Voltage Swing vs Output Current

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

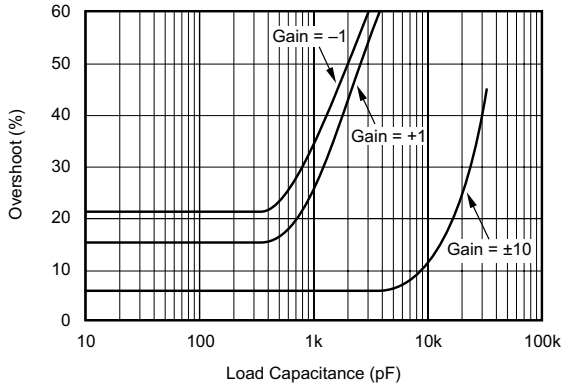


Figure 19. Small-Signal Overshoot vs Load Capacitance

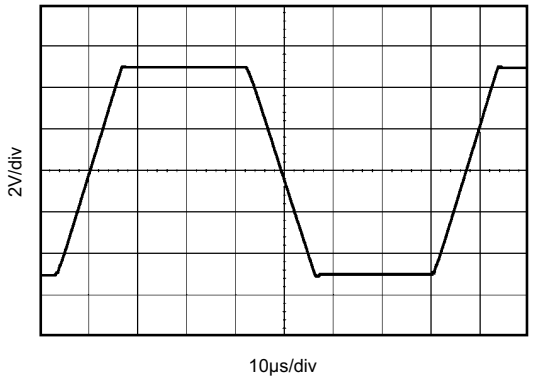


Figure 20. Large-Signal Step Response
G = 1, C_L = 1500 pF, V_S = ±15 V

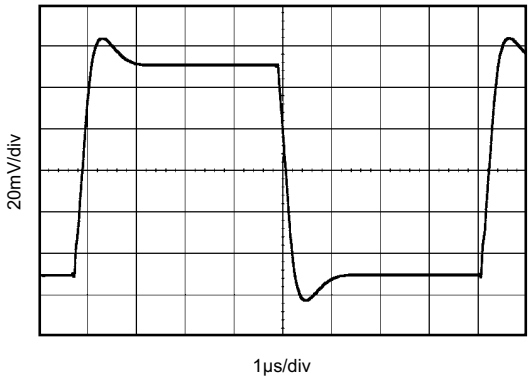


Figure 21. Small-Signal Step Response
G= +1, C_L = 0, V_S = ±15 V

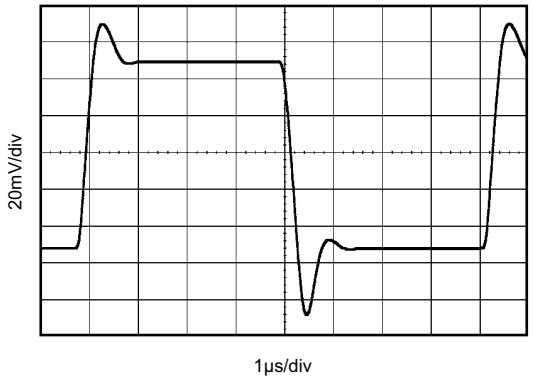


Figure 22. Small-Signal Step Response
G= 1, C_L = 1500 pF, V_S = ±15 V

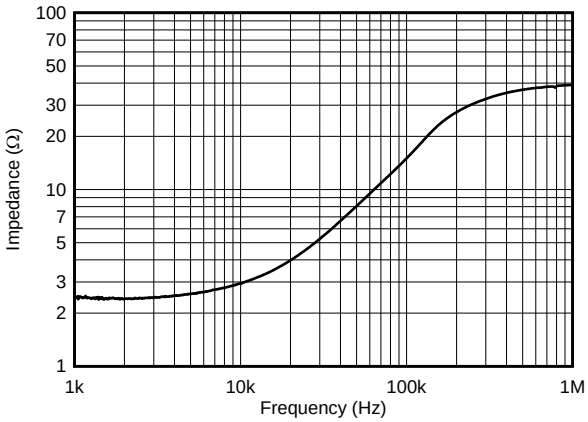


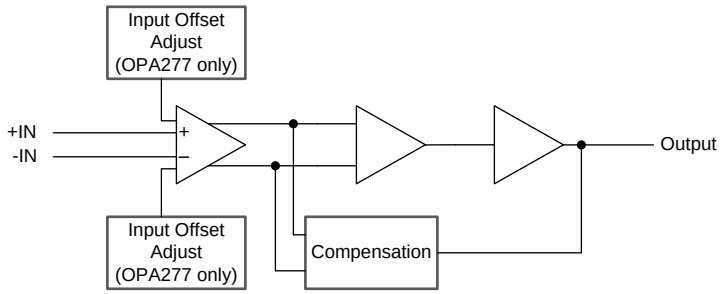
Figure 23. Open-Loop Output Impedance
V_S = ±15 V

7 Detailed Description

7.1 Overview

The OPAx277 series precision operational amplifiers replace the industry standard OP-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultralow offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications, for maximum design flexibility.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx277 series is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1-µF capacitors are adequate.

The OPAx277 series has low offset voltage and drift. To achieve highest performance, the circuit layout and mechanical conditions should be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPAx277 series. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections to the two input terminals similar
- Locate heat sources as far as possible from the critical input circuitry
- Shield operational amplifier and input circuitry from air currents, such as cooling fans

7.3.1 Operating Voltage

OPAx277 series operational amplifiers operate from ±2-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers, which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the ±5-V to ±15-V supply range. This allows a customer operating at V_S = ±10 V to have the same assured performance as a customer using ±15-V supplies. In addition, key parameters are assured over the specified temperature range, –40°C to 85°C. Most behavior remains unchanged through the full operating voltage range (±2 V to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in *Typical Characteristics*.

7.3.2 Offset Voltage Adjustment

The OPAx277 series is laser-trimmed for low offset voltage and drift, so most circuits do not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer, as shown in Figure 24. Only use this adjustment to null the offset of the operational amplifier. This adjustment should not be used to compensate for offsets created elsewhere in a system, because this can introduce additional temperature drift.

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Feature Description (continued)

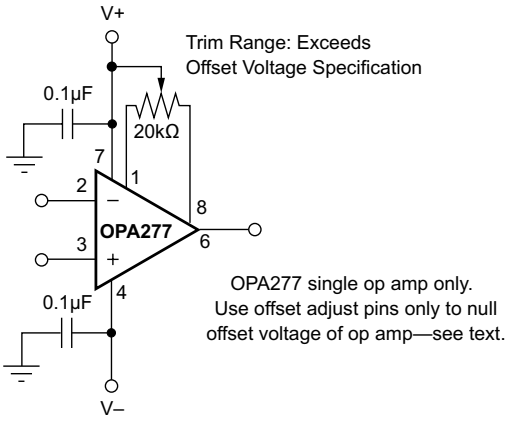


Figure 24. OPA277 Offset Voltage Trim Circuit

7.3.3 Input Protection

The inputs of the OPAx277 series are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are over-driven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

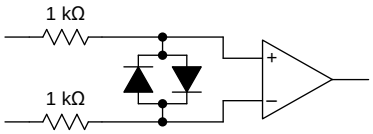


Figure 25. OPAx277 Input Protection

7.3.4 Input Bias Current Cancellation

The input stage base current of the OPAx277 series is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see Figure 26). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

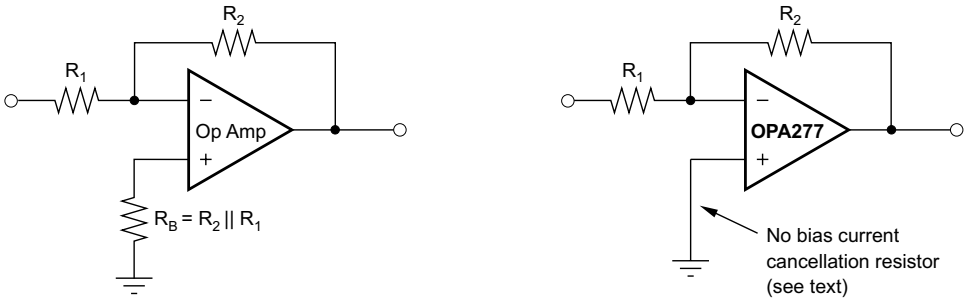


Figure 26. Input Bias Current Cancellation

Feature Description (continued)

7.3.5 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed circuit board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download at www.ti.com. The EMIRR IN+ of the OPA277 is plotted versus frequency as shown in Figure 27.

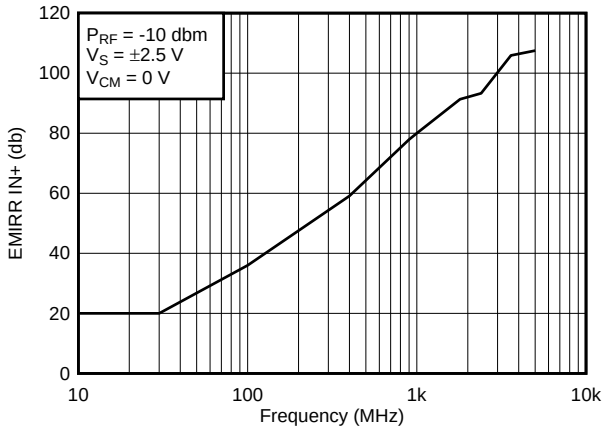


Figure 27. OPA277 EMIRR IN+ vs Frequency

If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA277 unity-gain bandwidth is 1 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

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Feature Description (continued)

Table 1 shows the EMIRR IN+ values for the OPA277 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA277 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	59.1 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	77.9 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	91.3 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio/satellite, S-band	93.3 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	105.9 dB
5.0 GHz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	107.5 dB

7.3.5.1 EMIRR IN+ Test Configuration

Figure 28 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). Note that a large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy. Refer to SBOA128 for more details.

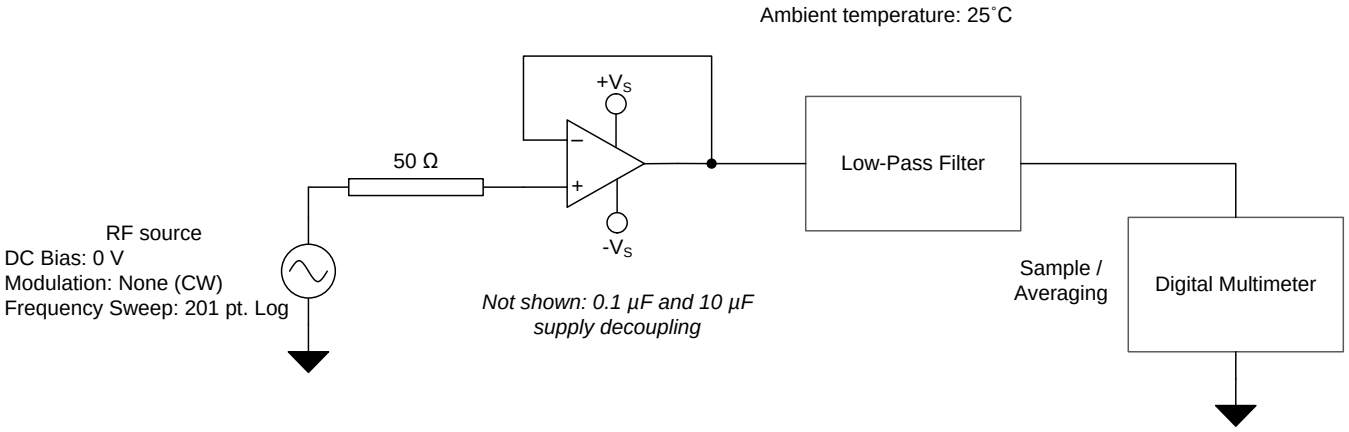


Figure 28. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

The OPAx277 has a single functional mode and is operational when the power-supply voltage is greater than 4 V (±2 V). The maximum power supply voltage for the OPAx277 is 36 V (±18 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx277 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer ultralow offset voltage and offset voltage drift, as well as 1-MHz bandwidth and high capacitive load drive. These features make the OPAx277 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Second-Order Lowpass Filter

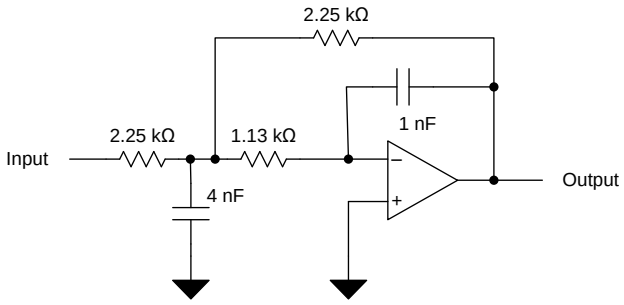


Figure 29. Second-Order Lowpass Filter

8.2.1.1 Design Requirements

- Gain = 1 V/V
- Lowpass cutoff frequency = 50 kHz
- –40 db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

8.2.1.2 Detailed Design Procedure

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

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Typical Applications (continued)

8.2.1.3 Application Curve

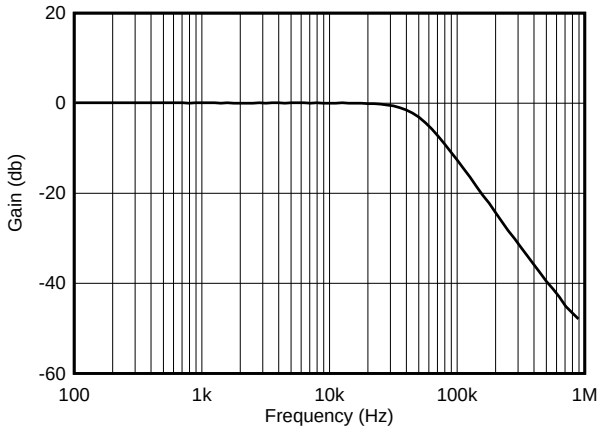
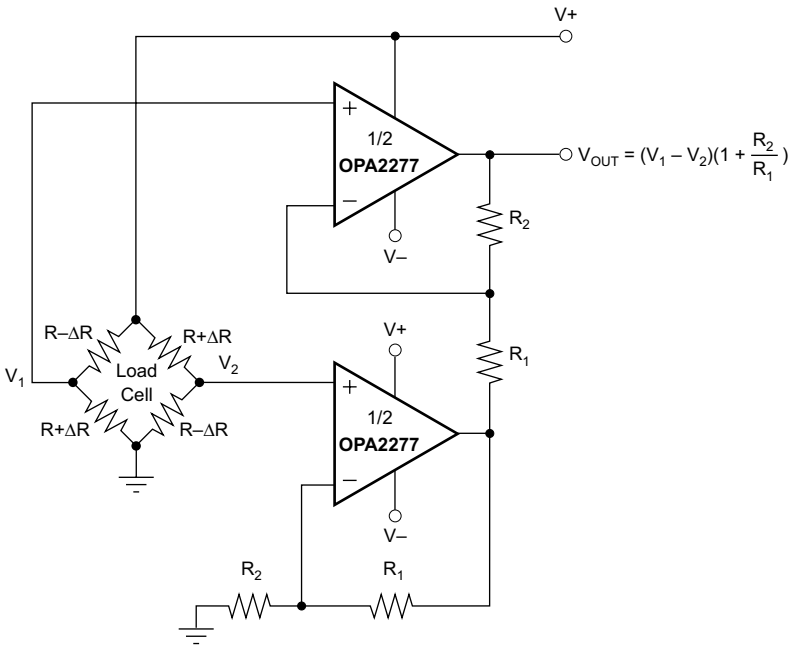


Figure 30. OPA277 Second-Order 50-kHz, Lowpass Filter

8.2.2 Load Cell Amplifier



For integrated solution see: INA126, INA2126 (dual)
INA125 (on-board reference)
INA122 (single-supply)

Figure 31. Load Cell Amplifier

Typical Applications (continued)

8.2.3 Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

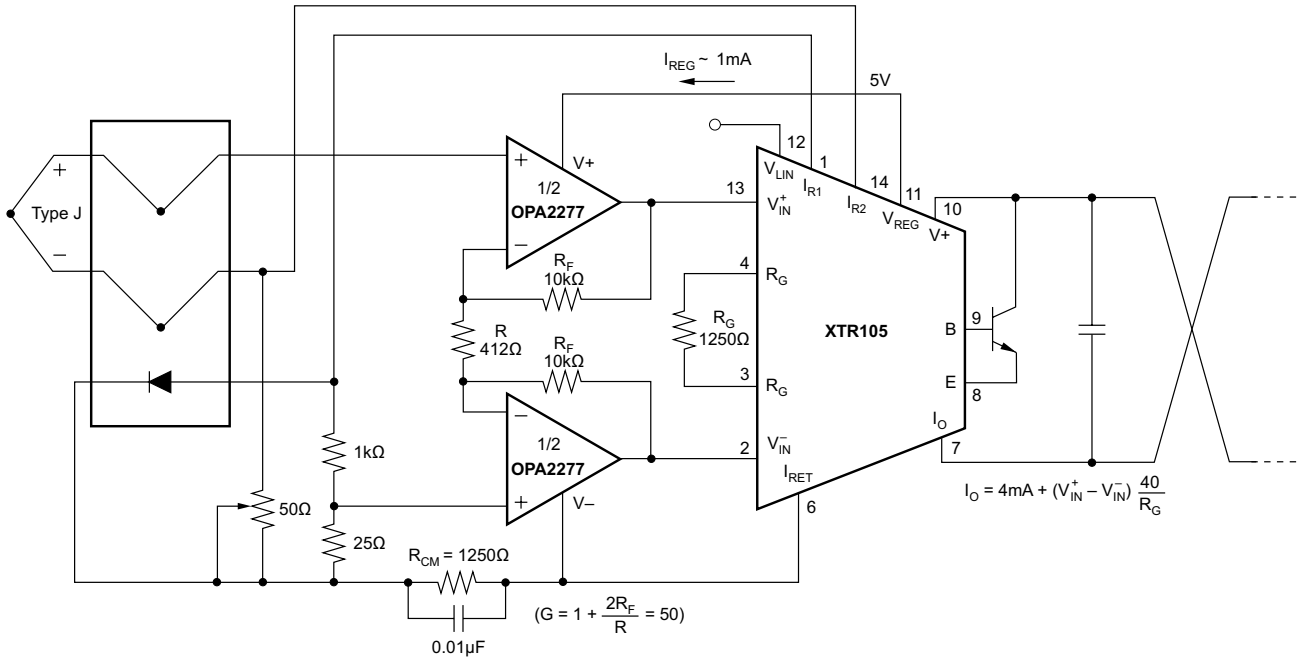


Figure 32. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

9 Power Supply Recommendations

The OPAx277 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 36 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

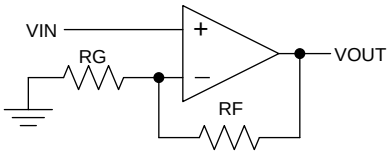
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

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Layout Guidelines (continued)

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- (DFN package only) The leadframe die pad should be soldered to a thermal pad on the PCB. The mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad.
- (DFN package only) Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long term reliability.

10.2 Layout Example



(Schematic Representation)

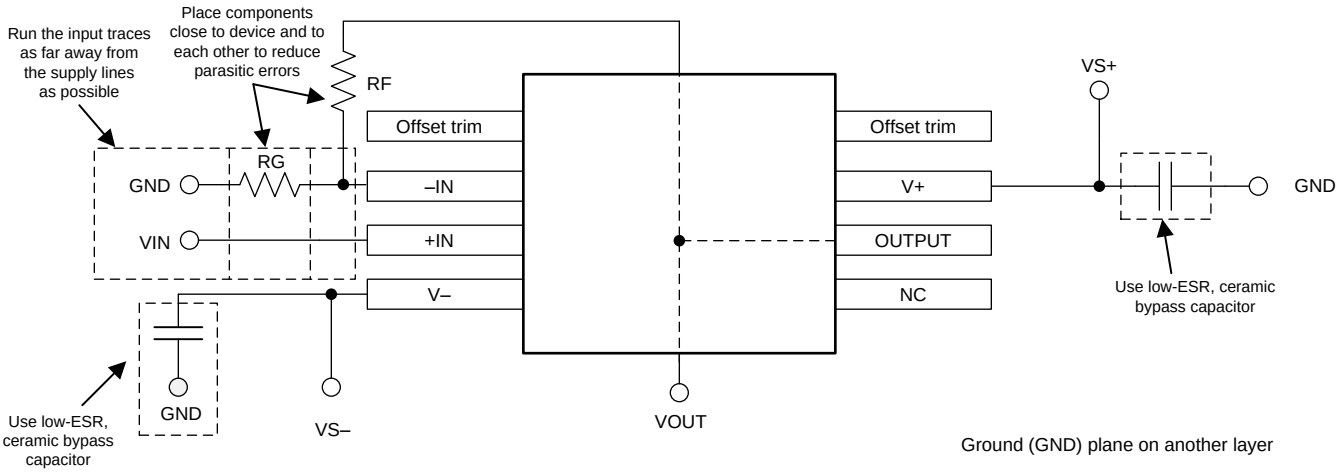


Figure 33. OPA277 Layout Example for the Noninverting Configuration

10.3 DFN Package

The OPAx277 series uses the 8-lead DFN (also known as SON), a QFN package with contacts on only two sides of the package bottom. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed-circuit-board (PCB) assembly techniques. See *QFN/SON PCB Attachment* (SLUA271) and *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to V–.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 WEBENCH Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

11.1.1.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.3 TI Precision Designs

The OPA277 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *QFN/SON PCB Attachment*, SLUA271
- *Quad Flatpack No-Lead Logic Packages*, SCBA017
- *EMI Rejection Ratio of Operational Amplifiers*, SBOA128
- *Circuit Board Layout Techniques*, SLOA089

11.2.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA277	Click here	Click here	Click here	Click here	Click here
OPA2277	Click here	Click here	Click here	Click here	Click here
OPA4277	Click here	Click here	Click here	Click here	Click here

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11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2277AIDRMT	ACTIVE	VSON	DRM	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		BHZ	Samples
OPA2277AIDRMTG4	ACTIVE	VSON	DRM	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		BHZ	Samples
OPA2277P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA2277P	Samples
OPA2277PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA2277P A	Samples
OPA2277PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA2277P A	Samples
OPA2277U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		OPA 2277U	Samples
OPA2277U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U	Samples
OPA2277U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U	Samples
OPA2277UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U A	Samples
OPA2277UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2277U A	Samples
OPA2277UA/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2277U A	Samples
OPA2277UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U A	Samples
OPA2277UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U A	Samples
OPA2277UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 2277U	Samples
OPA277AIDRMR	ACTIVE	VSON	DRM	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		NSS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA277AIDRMT	ACTIVE	VSON	DRM	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		NSS	Samples
OPA277P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA277P	Samples
OPA277PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA277P A	Samples
OPA277PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		OPA277P A	Samples
OPA277U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		OPA 277U	Samples
OPA277U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		OPA 277U	Samples
OPA277U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		OPA 277U	Samples
OPA277UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 277U A	Samples
OPA277UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 277U A	Samples
OPA277UA/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 277U A	Samples
OPA277UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 277U A	Samples
OPA277UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	OPA 277U A	Samples
OPA277UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		OPA 277U	Samples
OPA4277PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA4277PA	Samples
OPA4277UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4277UA	Samples
OPA4277UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4277UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4277UA/2K5E4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4277UA	Samples
OPA4277UAE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4277UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2277, OPA4277 :

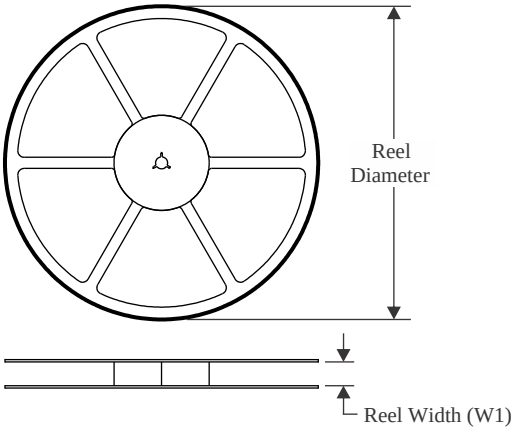
- Enhanced Product : OPA2277-EP, OPA4277-EP
- Space : OPA4277-SP

NOTE: Qualified Version Definitions:

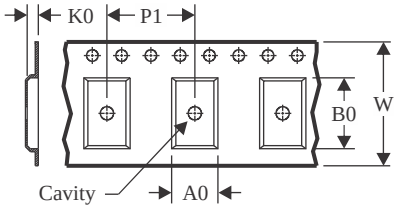
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

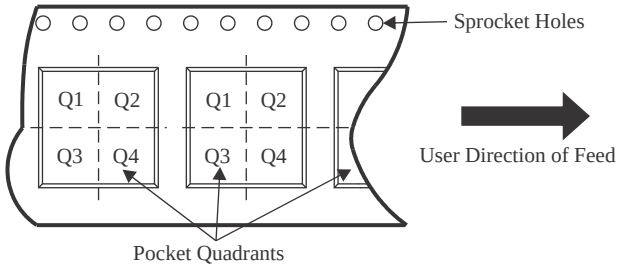


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

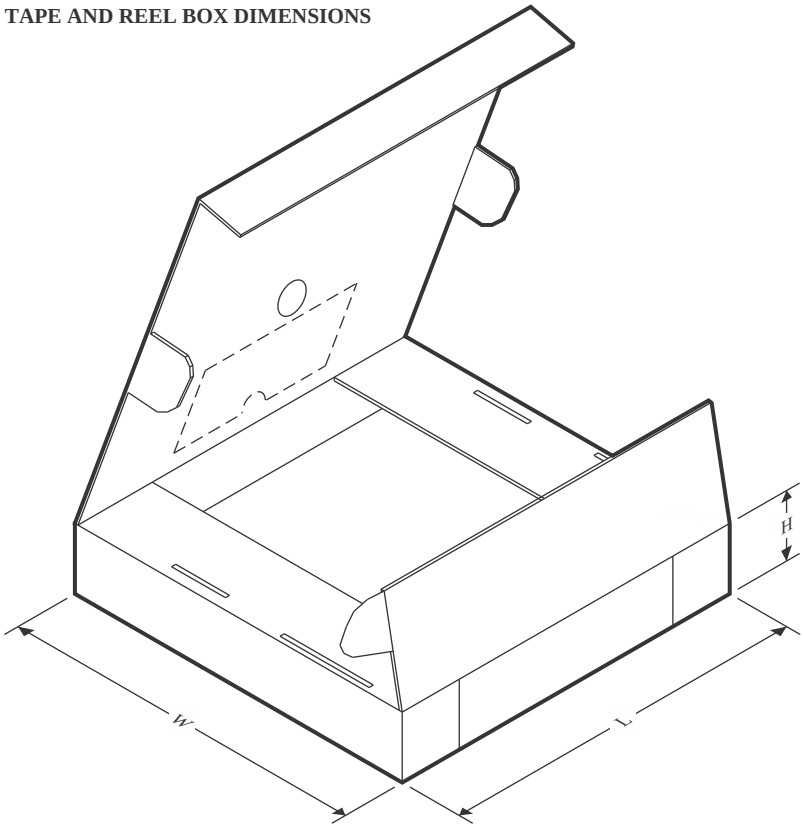
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2277AIDRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2277U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2277UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA277AIDRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA277AIDRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA277U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA277UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4277UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

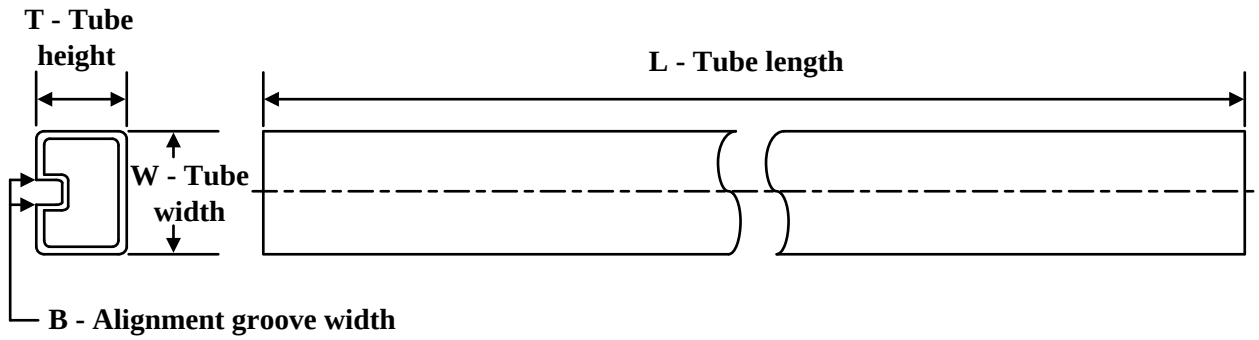
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2277AIDRMT	VSON	DRM	8	250	210.0	185.0	35.0
OPA2277U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2277UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA277AIDRMR	VSON	DRM	8	3000	356.0	356.0	35.0
OPA277AIDRMT	VSON	DRM	8	250	210.0	185.0	35.0
OPA277U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA277UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4277UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

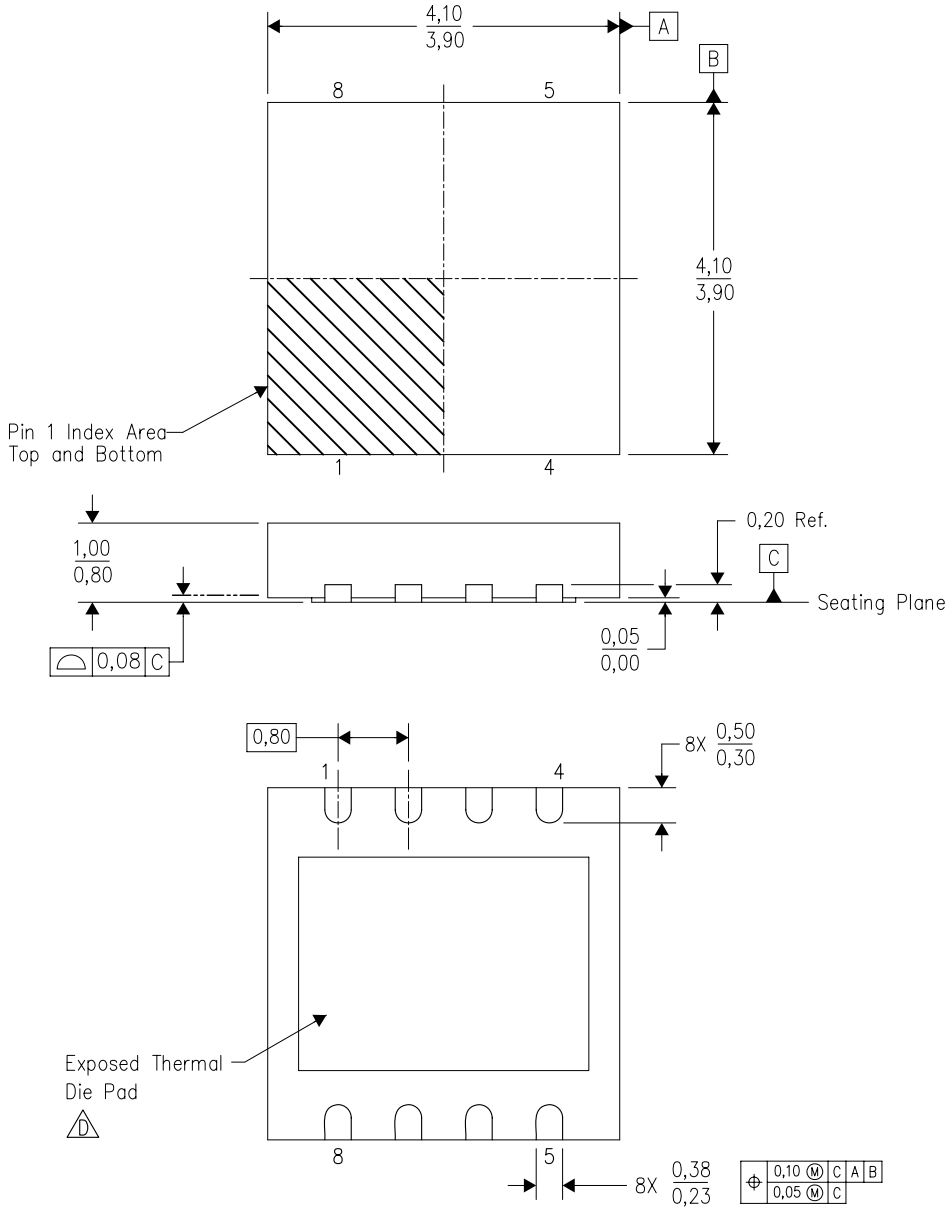
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2277P	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2277U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UAE4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UAE4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2277UG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA277P	P	PDIP	8	50	506	13.97	11230	4.32
OPA277PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA277PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA277U	D	SOIC	8	75	506.6	8	3940	4.32
OPA277UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA277UAE4	D	SOIC	8	75	506.6	8	3940	4.32
OPA277UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA277UG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA4277PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4277UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4277UAE4	D	SOIC	14	50	506.6	8	3940	4.32

DRM (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

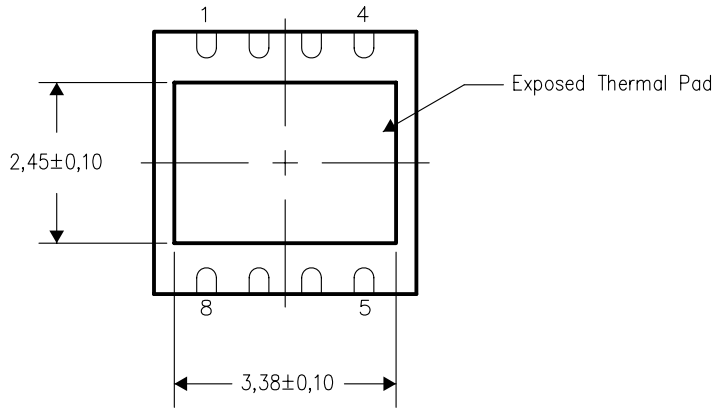
DRM (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

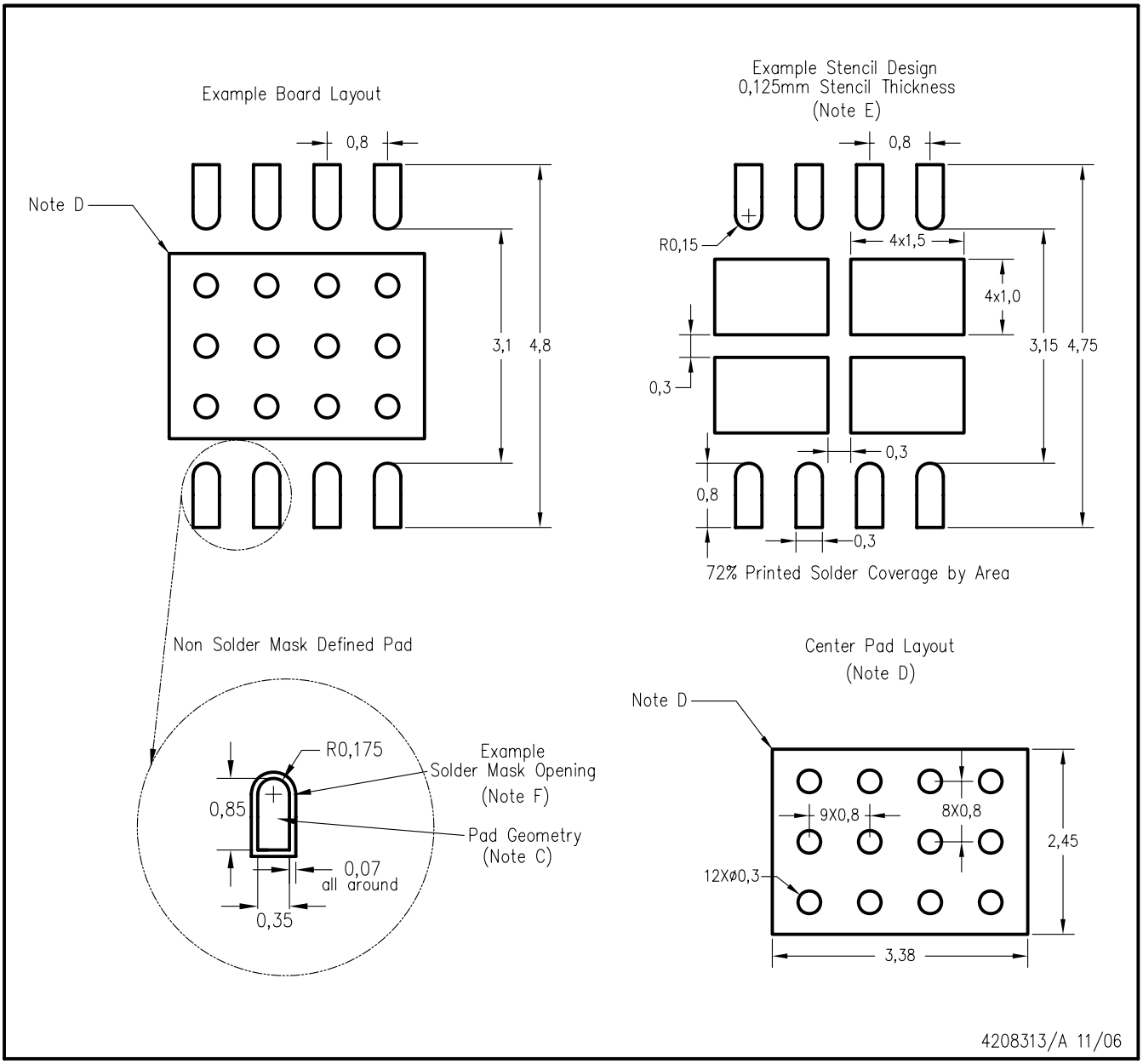


Bottom View

NOTE: All linear dimensions are in millimeters

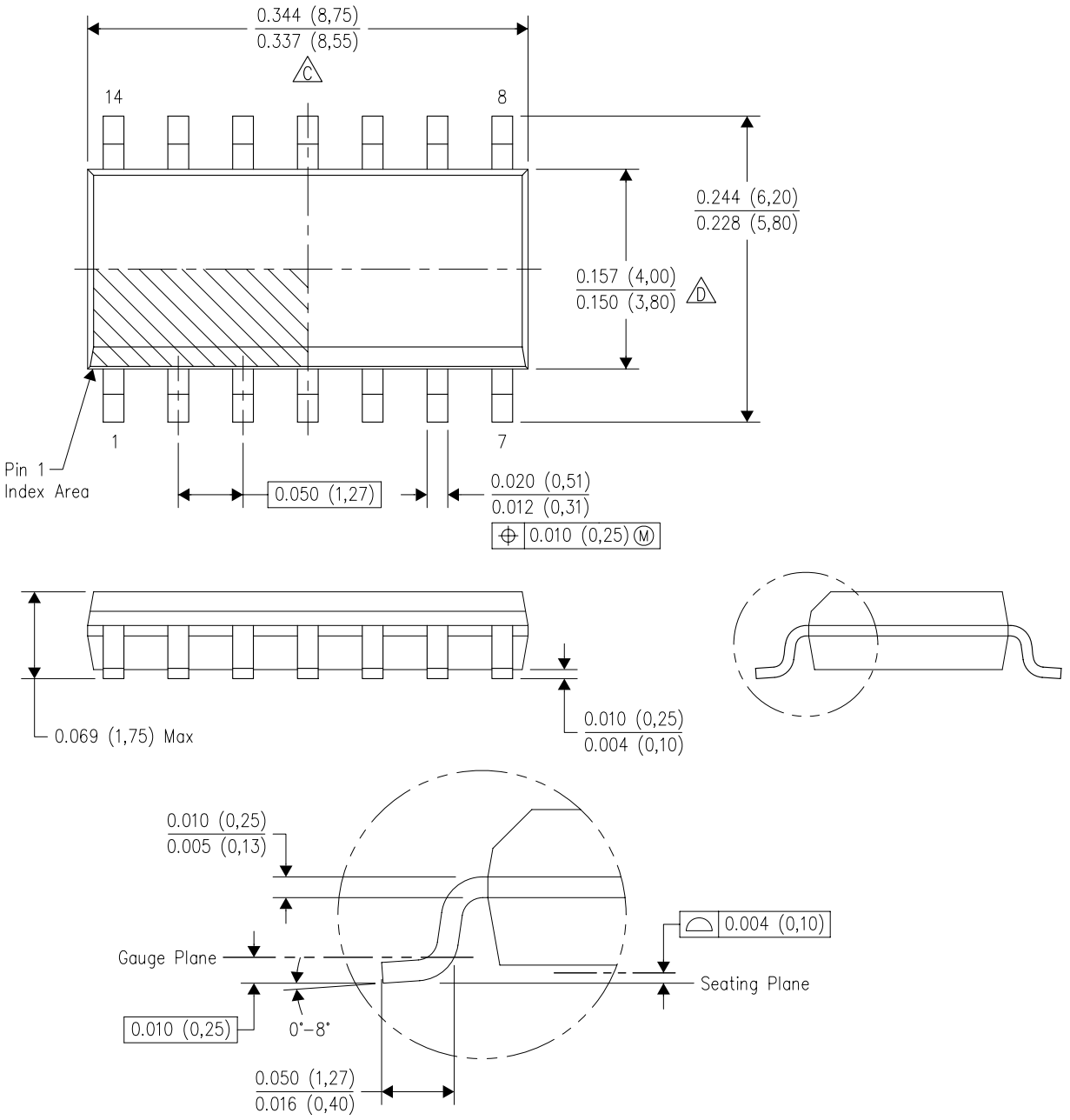
Exposed Thermal Pad Dimensions

DRM (S–PDSO–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

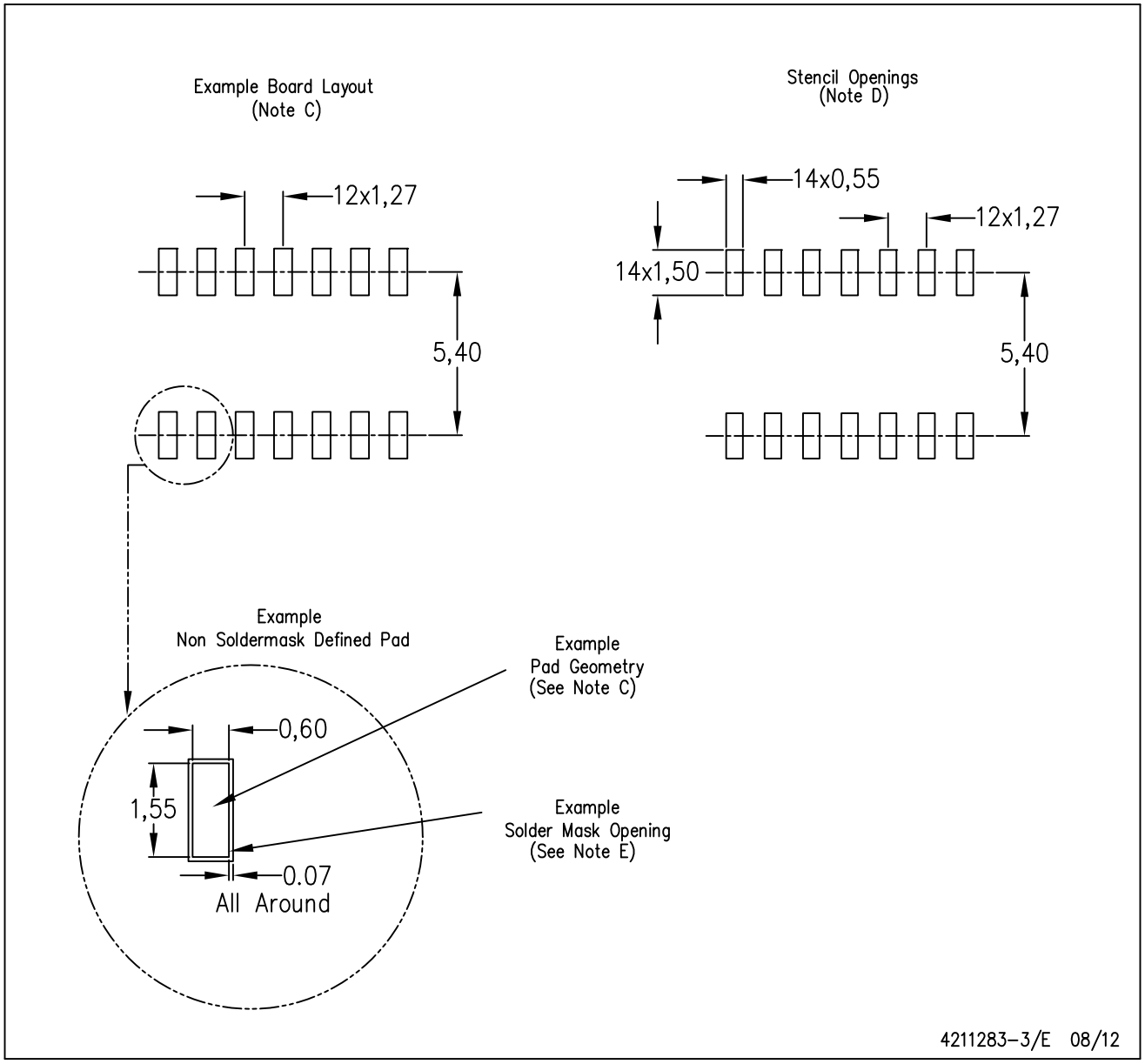
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



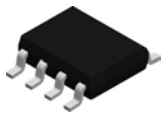
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

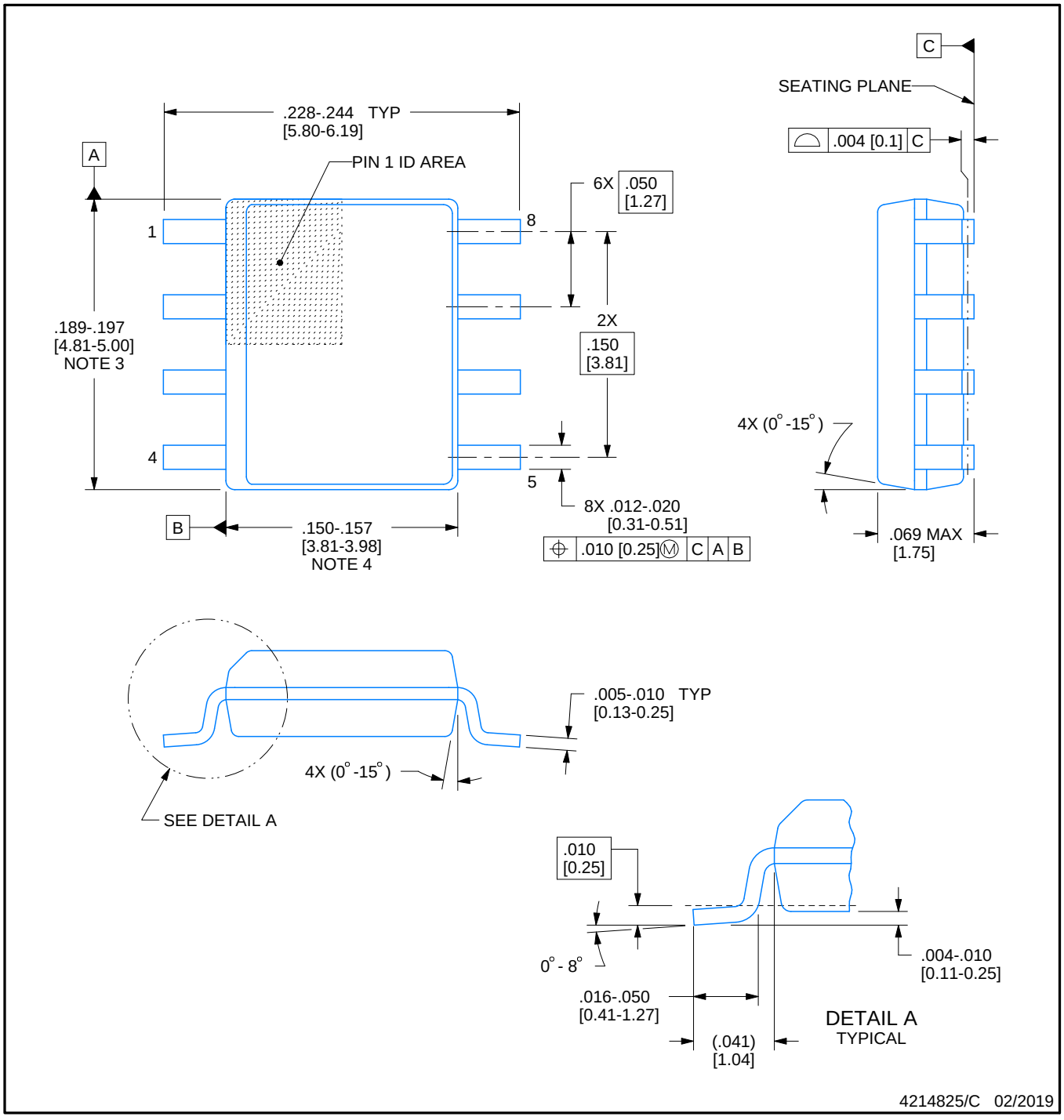


PACKAGE OUTLINE

D0008A

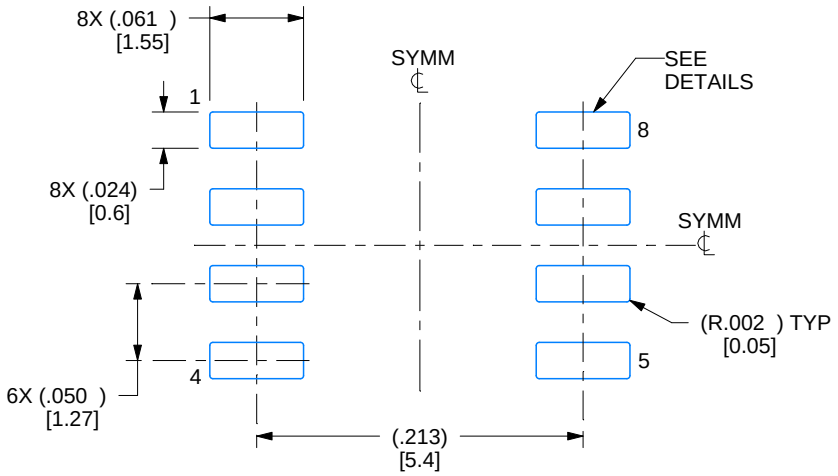
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

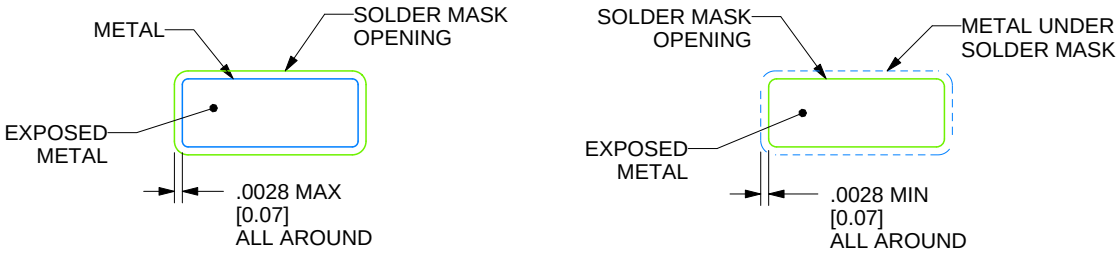


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

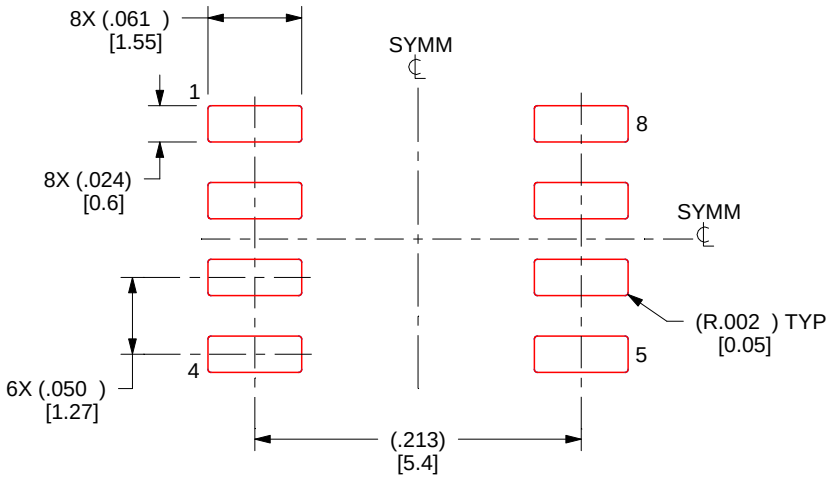
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



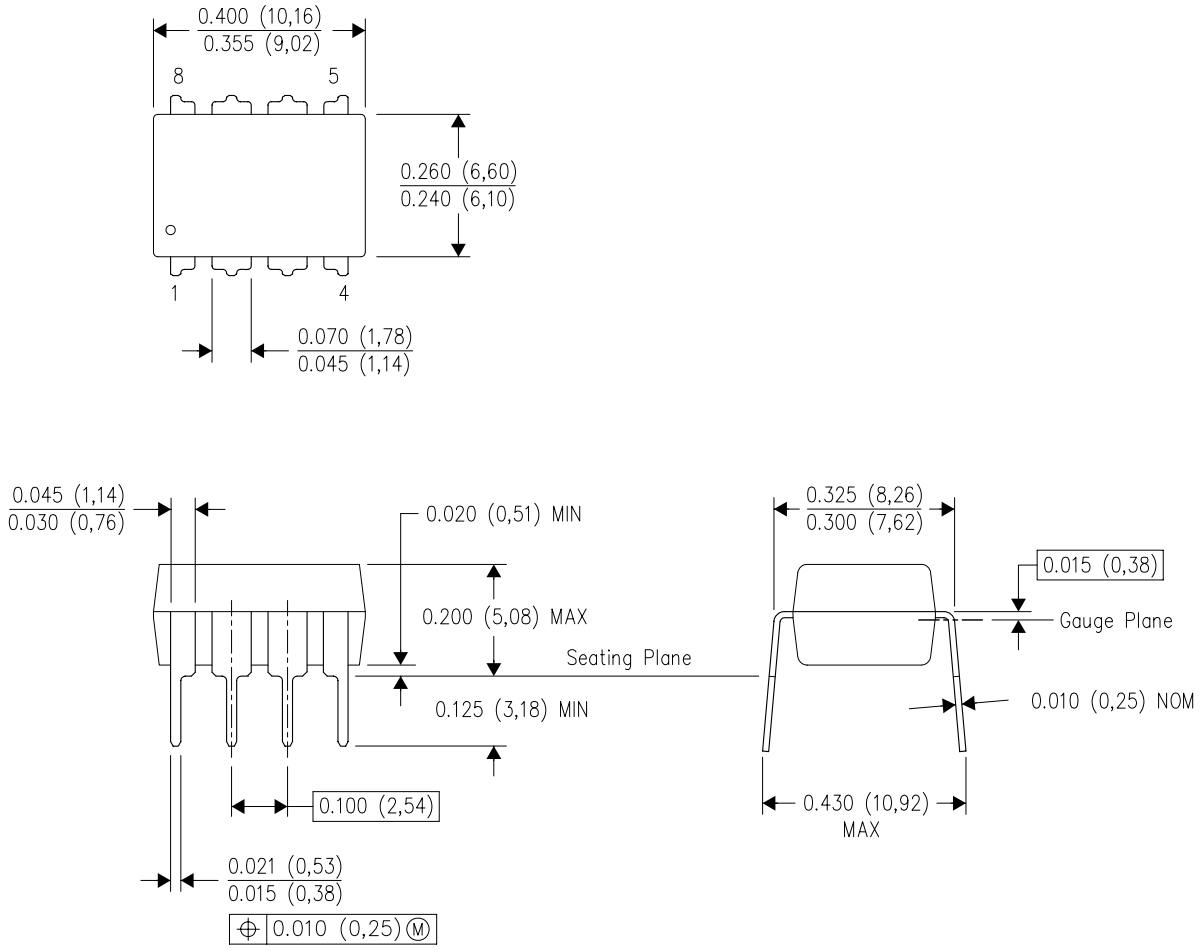
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

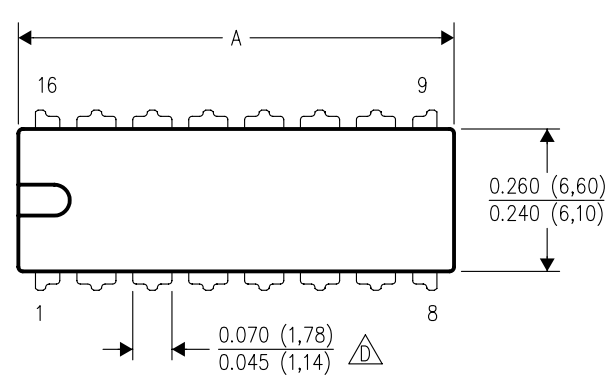


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

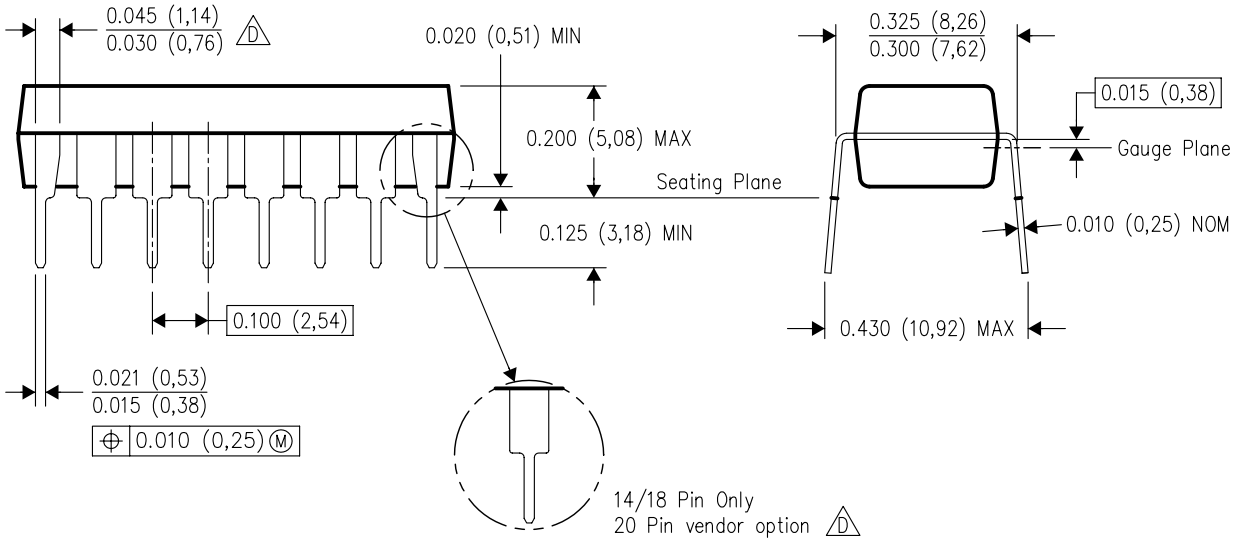
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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