AN2924

KSZ9031MNX to KSZ9131MNX Migration Guide

Author: *John MacKay*
Microchip Technology Inc.

INTRODUCTION

This document is intended for customers with an existing KSZ9031MNX board design migrating to the KSZ9131MNX for their board design. This includes hardware differences and software register differences between the two. Details for the hardware and software of each device can be found on the corresponding product page on the Microchip website.

Table 1 summarizes the hardware attribute differences between the KSZ9031MNX and the KSZ9131MNX. Table 2 summarizes the register differences between the KSZ9031MNX and the KSZ9131MNX.

TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9031MNX AND KSZ9131MNX

Device Attribute	KSZ9031MNX	KSZ9131MNX
TXD4, TXD5, TXD6, and TXD7 - MII mode	In MII mode, these pins are unused and can be driven high or low.	These pins are unused and can be driven high or low. If not driven, these signals require external pull-down resistors.
GTX_CLK - MII mode	Nothing mentioned.	If this pin is not driven, this requires an external pull-down resistor.
CRS and COL	Nothing mentioned about Duplex mode.	Used in Half-duplex mode only.
MODE Strapping Pins - MODE[3:0]	• 1001: Not used • 1011: Not used	• 1001: PME Enable on LED1/PME_N1. GMII mode - Advertise all capabilities (10-/100-/1000-speed half-/full-duplex), except 1000BASE-T half-duplex. • 1011: PME Enable on INT_N/PME_N2. GMII mode - Advertise all capabilities (10-/100-/1000-speed half-/full-duplex), except 1000BASE-T half-duplex.
ALL-PHYAD	No functionality	Pin 53 can be set to respond to the KSZ9131 PHY Address (from PHYAD[2:0]) and PHY Address 0.
Energy Efficient Ethernet (EEE)	No functionality	Supports EEE.
LED modes	Single and Tri-Color	Single, Tri-Color, and Enhanced. Enhanced LED mode has more controls for LED function.
Dynamic Channel Quality	No functionality	Dynamic Channel Quality Features: • Mean Square Error (MSE) • Signal Quality Indicator (SQI) • Peak Mean Square Error (pMSE)
ISET Resistor	12.1 kΩ	6.04 kΩ

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TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9031MNX AND KSZ9131MNX

Register	KSZ9031MNX	KSZ9131MNX
6h	Bit[6:5] - Reserved	• Bit 6: Receive Next Page Location Able • Bit 5: Received Next Page Storage Location
9h	Bit 8 can be set to advertise PHY is 1000BASE-T half-duplex capable.	Bit 8 should be set to 0 to advertise PHY is not 1000BASE-T half-duplex capable. The KSZ9131MNX does not support this mode.
12h	Bits[7:0] - For the open or short cable fault detected in Bits[9:8] of this register, this 8-bit value represents the distance to the cable fault.	Bits[7:0] - When VCT_SEL = 00, this is the data of cable diagnostics. Valid only when VCT_EN = 0. • If cable is normal (that is, VCT_ST = 00), VCT_-DATA is “don’t care”. • If cable is open or short (that is, VCT_ST = 01 or VCT_ST = 10), the distance to the fault is approximately 0.8 * (VCT_DATA - 22) (in meters). • If cable diagnostics failed (that is, VCT_ST = 11): - Bit[7] = 1 means invalid reflected pulse width, that is, equal or greater than 152 ns, equal or less than 48 ns. - Bit[6] = 1 means the cable has signal for too long time during WAIT state. It is unusual and for debug only. - Bit[5] = 1 means mask100 is detected and no silent time window can be found for diagnostics. It means high frequency signal is found on the line. The link partner probably is in forced 100BT or 1000BT mode. - Bit[4] = 1 means that signals faster than NLP and FLP exist and no silent time window can be found for diagnostics. It is unusual and for debug only. - Bit[3:2] = number of low pulses detected. If more than 3, stay at 3. - Bit[1:0] = number of high pulses detected. If more than 3, stay at 3.
13h	Bits[15:3] - Reserved • Bit 2 - 1000BASE-T Link Status • Bit 1 - 100BASE-TX Link Status • Bit 0 - Reserved	Bits[15:2] - Reserved • Bit 1 - 1000BASE-T Link Status • Bit 0 - 100BASE-TX Link Status
16h	Reserved	• Bits[15:8] - Reserved • Bits[7:4] - LED2 Configuration • Bits[3:0] - LED1 Configuration
17h	Reserved	• Bits 15, 13, [9:7], [4:2] - Reserved • Bit 14 - LED Activity Output Select • Bit 12 - LED Pulsing Enable • Bits[11:10] - LED Blink/Pulse Stretch Rate • Bits[6:5] - LED Pulse Stretch Enable • Bits[1:0] - LED Combination Disable
19h	Reserved	• Bits 15 - Reserved • Bit 1 - MDIO Drive • Bit 0 - Reserved

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TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9031MNX AND KSZ9131MNX (CONTINUED)

Register	KSZ9031MNX	KSZ9131MNX
1Ah	Reserved	• Bit 15 - Reserved • Bit 14 - KSZ9131 LED mode • Bits[13:0] - Reserved
1Dh	Reserved	• Bits[15:12], [9:0] - Reserved • Bit 11 - spd_clock_gate_override • Bit 10 - spd_pll_disable
1Eh	Reserved	• Bits[15:4],[2:0] - Reserved • Bit 3 - External Loopback Enable
1Fh	Bits 8 and 1 - Reserved	• Bit 8 - Enable SQE Test • Bit 1 - Software Reset
Address 0, Reg 3h	AN FLP Burst Transmit - LO	Reserved
Address 0, Reg 4h	AN FLP Burst Transmit - HI	Reserved
Address 1, Reg 5Ah	• Bits[15:4] - Reserved • Bits[3:1] - 1000BASE-T Link-Up Time • Bit 0 - Reserved	Reserved
Address 2, Reg 0h	• Bits[15:5], 2, 0 - Reserved • Bit 4 - LED mode override • Bit 3 - Single LED • Bit 1 - 125 MHz Clock Enable	• Bits[15:5], [3:2] - Reserved • Bit 4 - Single LED • Bit 1 - 125 MHz Clock Enable • Bit 0 - All-PHYAD Enable
Address 2, Reg 2h	• Bits[15:11], [9:7], [6:5], [3:2], 0 - Reserved • Bit 10 - PME_N2 Output Enable • Bit 4 - NAND Tree Strap Override • Bit 1 - GMII/MII Strap Override	• Bits[15:12], 10, [8:5], [3:2], 0 - Reserved • Bit 11 - GMII mode with PME_N2 mapped to INT_N • Bit 9 - GMII mode with PME_N1 mapped to LED1 • Bit 4 - NAND Tree Strap Override • Bit 1 - GMII/MII Strap Override
Address 2, Reg 3h	• Bits[15:7], [6:5], [3:2], 0 - Reserved • Bit 4 - NAND Tree Strap Status • Bit 1 - GMII/MII Strap Override	• Bits[15:12], 10, [8:5], [3:2], 0 - Reserved • Bit 11 - GMII mode PME_N2 Strap Status • Bit 9 - GMII mode with PME_N1 Strap Status • Bit 4 - NAND Tree Strap Status • Bit 1 - GMII/MII Strap Status
Address 1Ch, Reg 4h	• Bits[15:11], [9:0] - Reserved • Bit 10 - 10BASE-Te mode	Reserved
Address 1Ch, Reg 9h	Reserved	• Bits [15:10], [8:0] - Reserved • Bit 9 - 10BASE-Te mode

Additional features such as EEE, MSE/SQI, and Self-Test for Frame Generation/Checking are accessible in the Indirect Address Registers.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002924A (01-30-19)	Initial release.	

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